Remarks

Claims 1-9 are pending in the application. No amendments have been made to the claims. The title of the invention has been amended to recite, "DUAL MODE CMOS INTEGRATED IMAGER HAVING USER INTERFACE." Reconsideration is respectfully requested.

Objection to the Specification

In the Office action, the Examiner states that the title of the invention is not descriptive and that a new title is required that is clearly indicative of the invention. Applicants submit that the title has been amended to recite, "DUAL MODE CMOS INTEGRATED IMAGER HAVING USER INTERFACE." Therefore, the objection to the title should be withdrawn.

Rejections Under 35 U.S.C. § 103

Claims 1-6

Claims 1-6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Shinohara in view of Noble et al. This rejection is respectfully traversed.

With regard to Shinohara the Examiner states, "Shinohara does not teach the interface as a user interface configured to receive the mode signal from user." Office action, at 3. The Examiner continues by stating that Noble et al. supplement the missing teaching of Shinohara. Specifically, with regard to Noble et al., the Examiner provides:

> Noble et al. teach (see Fig. 1) a microprocessor (10) with a user interface (12) wherein the clock frequency ("Clock Frequency") is adjusted based on a mode signal (SLOW#) received from a user (see Col. 3, lines 46-49 and Col. 6, lines 21-29) to provide user control of power consumption (See Col. 6, lines 24-29). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a user interface receiving a mode

> signal from a user as taught by Noble et al. in the system of Shinohara, to provide customized user control of power consumption to best suit a user's particular needs, as taught by Noble et al. (see Col. 6, lines 24-29). Office action, at 3-4.

Applicants submit that Shinohara either alone, as will be described below with regard to claims 7-9, or in combination with Noble et al. fail to teach or suggest the claimed invention.

The Examiner states that the missing teachings of Shinohara are supplemented by Noble et al. Applicants respectfully disagree. Noble et al. were concerned with a method for adjusting a clock frequency and voltage supplied to a processor via two signal lines which may be user supplied. In Noble (Fig. 1), it is seen that a clock is coupled to and controls the frequency at which a processor operates. A voltage regulator is also coupled to the processor and determines the voltage at which the processor operates. Once the frequency of the clock is reduced, after receiving a SLOW_# signal which may be user sent, the frequency of the processor is reduced. The clock also communicates directly with the voltage regulator, telling the voltage regulator to lower the voltage supplied to the processor. The voltage operator complies, and the processor continues to operate in a low power mode. A POWER_READY signal received by the clock will raise the voltage.

Therefore, in Noble et al., the user provides a signal that lowers the frequency of the clock. The user signal <u>does not bypass the internal timing element to control timing operation of the system</u>. The signal merely raises or lowers the frequency of the clock, thus the frequency of the processor.

If the Noble et al. teaching were to be combined with the Shinohara teaching, a user of Shinohara would be able to control the amount of voltage supplied to a processor via a timing element. Noble et al. fails to provide any teaching or

suggestion that would direct one of skill in the art to provide a user signal that would cause the internal timing mode to be bypassed to control the timing operation of the system. Instead, Noble merely provides a teaching that would allow a user to decrease or increase the frequency of the clock, thus the voltage that would be supplied to a single processor. There is no teaching or suggestion in Noble to provide a user signal that would bypass the clock to control the timing operation of the system.

In contrast, the present invention is drawn toward a user interface receiving a user mode signal for setting the system in one of a first operating mode using an internal timing element or of a second operating mode bypassing the internal timing element to control the timing operation of the system. Specifically, claim 1 recites, "a user interface for receiving a plurality of… signals, said interface configured to receive from a user a user mode signal for setting the system in one of a first operating mode or a second operating mode characterized in that the first operating mode uses the internal timing element to control timing operation of the system and the second operating mode bypasses the internal timing element to control timing operation of the system."

Elements of Applicants' claim 1 are not taught or suggested by Shinohara or Noble et al. Therefore, the rejection to claim 1 should be withdrawn.

As claims 2-6 depend, either directly or indirectly upon claim 1, Applicants respectfully submit that the rejection to these claims should be withdrawn for at least the same reasons as claim 1.

Further, Noble et al. were concerned with a user controlling the frequency of a single timing element. Noble fails to teach or suggest that a user control whether an internal timing element is bypassed such that an external timing element controls the timing operation of the system.

Specifically, claim 3 recites, "[t]he imager system of claim 1, further including means for receiving timing signals from an external timing element when the system is operating in the second operating mode."

Claims 4 and 5, depend from claim 3 and are thus non obvious over the cited prior art for at least the reasons provided with regard to claim 2.

Claims 7-9

Claims 7-9 are rejected under 35 U.S.C. § 103(a) are rejected as being unpatentable over Shinohara. This rejection is respectfully traversed.

With regard to Shinohara, the Examiner states, "Shinohara do not teach a user establishing timing signals and a user interface allowing selection of the onboard timing means or outboard logic circuit." Office action, at 4. The Examiner continues, "[i]t would have been obvious for one of ordinary skill in the art at the time the invention was made to establish a user interface to allow selection of onboard timing means or outboard logic circuit and allow a user to establish timing signals in the timing selector of Shinohara, to allow user control of power consumption from the microprocessor and activation/deactivation of the image processing functions provided by the microprocessor to provide a more user-flexible system." Office action, at 5. Applicants respectfully disagree.

Shinohara was concerned with reducing power consumption in the solid state image pickup device by using a feedback mechanism wherein user control cannot be used. Shinohara provides a feedback mechanism whereby a switch is automatically shifted so that a signal from the microcomputer is supplied to the drive pulse generation circuit instead of a signal from the reference clock generation circuit and the preliminary operation mode generation circuit. Specifically, Shinohara recites, "[t]he signals read from the sensor unit

are entered into the image detection circuit, and, if the necessary image is detected, the output of the latch circuit is shifted to a high level state whereby the microcomputer is turned on. At the same time the switch 9 is shifted that the signal from the microcomputer is supplied to the drive pulse generation circuit." Shinohara, col. 4, lines 16-22. Additionally, Shinohara states:

> [I]n the preliminary operation, the preliminary operation mode generation circuit 8 generates a drive control signal of the preliminary operation mode based on the reference clock signal generated by the reference clock generation circuit 7 on the image sensor chip, and the drive pulse generation circuit 21 generates drive pulses based on the generated drive control signal to drive the peripheral scanning circuits. The image pickup unit sequentially reads out the image…. In the case that the image detection circuit 11 determines that the sensor receives the necessary image, the latch circuit 12 is latched. This determination may be attained by simple image detection, such as detection of an image signal component whose level is greater than a pre-determined level. In the preliminary operation, it is therefore possible in a scanning and read-out operation to reduce the number of horizontal and vertical scanning lines in image signal reading… or to perform the operation intermittently, since the sensor is operated as a monitor to merely determine whether or not the sensor receives the necessary image. The power consumption in this case can be significantly reduced not only in the microcomputer but also in the solid state image pickup device." Shinohara col. 4, line 46 to col. 5, lines 13 (emphasis added).

The Examiner states that it would have been obvious to establish a user interface to allow selection of onboard timing means or outboard logic circuit in Shinohara. However, Applicants respectfully submit that an object of Shinohara is to reduce power consumption through use of the automated feedback mechanism of the sensor. Therefore, if the feedback sensor of Shinohara were to be substituted with the "user interface allowing selection of the onboard timing means or

outboard logic circuit," as recited in claim 7, Applicants submit that the principle of operation of Shinohara would be altered. This is not permissible when making an obviousness determination. The MPEP explicitly articulates this rule as follows:

> If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. M.P.E.P. § 2143.01, 2100-125 (August 2001) (citing *In re Ratti*, 123 U.S.P.Q. 349 (CCPA 1959)).

Therefore, Shinohara does not suggest the claimed invention.

Further, Applicants respectfully submit that Shinohara fails to teach or suggest, as recited in Applicants' claim 7, "an outboard logic circuit electrically connected to the CMOS integrated imager generating signals established by a user for establishing user defined timing signals for customized imager operation…." There is no teaching or suggestion in Shinohara that provides that the user customizes an imager operation by establishing signals. Applicants respectfully submit that "[m]odification unwarranted by the disclosure of a reference is improper." Carl Schenck, A.G. v. Nortron Corp., 218 U.S.P.Q. 698, 702 (Fed. Cir. 1983).

Furthermore, an advantage of Applicants' invention is that "[t]he invention … provides the user the option to take control of every aspect of scan timing externally in an FPGA if the user requires the modes of operation to be extended for advanced imaging." Applicants' specification, at page 3, lines 21-24.

Therefore, Applicants respectfully submit that Shinohara fails to teach or suggest the present invention.

As claims 8-9 depend from claim 7, Applicants respectfully submit that the rejection to these claims should be withdrawn for at least the same reasons as claim 7.

Conclusion

For at least the reasons submitted above, Applicants respectfully submit that claims 1-9 are in condition for allowance. Accordingly, a Notice of Allowance is respectfully requested.

CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Asst. Commissioner for Patents, Washington, D.C. 20231

Signed: Sally Azevedo
Typed Name: Sally Azevedo

Date: April 9, 2003

Respectfully submitted,

Gina McCarthy

Gina McCarthy
Reg. No. 42,986

P.O. Box 2-E
San Jose, CA 95109-0005
(408) 297-9733